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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,384	03/09/2001	Lajos Gazsi	12816-006001/ S0816 GC/aj	7389

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FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
CHO, HONG SOL	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/803,384	GAZSI ET AL.	
	Examiner	Art Unit	
	Hong Cho	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 5-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to the RCE filed on 8/22/2005. Claims 2-4 were canceled. Claims 1 and 5-21 are pending in the instant application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7-12, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partridge et al (U.S 6160811), hereinafter referred to as Partridge, in view of Kudo (US 5278830), and further in view of Locklear et al (US 6252878), hereinafter referred to as Locklear.

Re claim 1, Partridge discloses a data packet router (*high-speed router*) in a communication network (*data networks*) for forwarding data packets with a header and a payload and multiple independent forwarding processors for processing header data (*a plurality of data processing processors for parallel data processing of the header data*, column 1, lines 4-8; column 2, lines 14-15). Partridge discloses sending the headers to a

selected forwarding engine by the receiving TSU (to-switch-unit), which buffers the payload of the packet (*a demultiplexer for separating the data packets into header and useful data*, column 4, lines 9-11). Partridge fails to teach distributing the header data based on the priority of the header data and the workload of the data processing processors. However, Kudo discloses distributing the packet according to the priority data of header data (column 2, lines 38-43) and Locklear discloses directing information to a selected route processor based on its loading characteristics (column 1, lines 43-49). It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the teachings of Kudo and Locklear into Partridge for distributing the packet based on the priority of the header data and the workload of the data processing processors to provide the optimized management of packet distribution by meeting quality of service and avoiding work overloading of a given processing processor.

Re claim 7, Partridge discloses a packet received and buffered at the line interface TSU (*a useful data memory is provided for buffer storing the separated useful data*, column 5, lines 21-22).

Re claim 8, Partridge provides a process to provide a respective identifier to the header data and useful data to be reassembled into packets (column 6, lines 33-36).

Re claims 9 and 10, Partridge discloses TSU page processor (*a first and second multiplexer*) merging the header and payload buffered (*coming from the useful data memory*) from TSU (*compiling header data and useful data*, column 4, lines 8-10; column 6, lines 29-34).

Re claim 11, Partridge discloses TSU page processor with FIFO memory for transmitting the header and payload to the outgoing line interface card (*the first multiplexer has a FIFO memory connected downstream of it for outputting the compiled data packets through the router*, column 6, lines 27-30).

Re claim 12, Partridge discloses TSU page processor (element 155, figure 3b) connected to the switch interface (element 159, figure 3b) (*the output of the second multiplexer is connected to the switching mechanism*).

Re claim 14, it is inherent that each processor has a dedicated memory for the purpose of transferring data in memory.

Re claim 17, Partridge discloses TSU that buffers payload of the packet (*the demultiplexer has an input buffer connected upstream of it*, column 4, lines 9-11).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Partridge in view of Kudo and Locklear and further in view of Bremer et al (U.S 6032190), hereinafter referred to as Bremer.

Re claim 5, Partridge fails to teach explicitly the header data being distributed to the data processing processors by means of DMA operations. Bremer, however, teaches transferring the header portion of the data packet to a packet processor unit by DMA controller. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use DMA controller of Bremer in distributing the header data to the data processing since a DMA controller controls data transfer between the various components within the system memory (column 5, lines 27-32).

Claims 6, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partridge in view of Kudo and Locklear and further in view of Cooperman et al (U.S 5721833), hereinafter referred to as Cooperman.

Re claims 6 and 16, Patridge fails to teach a CAM processor connected to the FIFO memory through a bus having an associative memory for classifying the data packets. Cooperman, however, teaches writing (*having an associative memory*) each cell (*data packet*) with priority into a CAM (column 2, lines 41-44). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a CAM processor of Cooperman in classifying data packets since CAM provides comparison logic in reconstructing information stored in memory.

Re claim 13, Partridge discloses processors connected to each other through a bus (*distribution processor, data processing processors, and the CAM processors are connected to a common data bus*, column 3, lines 53-56).

Re claim 15, Partridge discloses all of the limitation of the base claim, but fails to teach explicitly a common memory connected to the header data bus. **Official notice is taken** that a memory component is connected to the data bus such as PCI bus.

Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partridge.

Re claims 18, 19 and 21, Partridge discloses all of the limitation of the base claim, but fails to teach explicitly a high-speed router used in LANs or Internet. **Official notice**

is taken that routers are used to forward data packets between networks such as LANs, WANs, and Internet.

Re claim 20, Partridge teaches forwarding engines employing the same processor type (column 4, lines 36-37). Partridge fails to teach explicitly using the same processor type for the distribution processor as used in the data processing processors. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use same processor type for the distribution processor as used in the data processing processors to get design compatibility among processors.

Response to Arguments

4. Applicant's arguments filed on 8/22/2005 have been fully considered but they are not persuasive.

On page 6 the Applicant argues that Kudo does not disclose or suggest separating the packets into header data and useful data and distributing the separated header data at least in part on the basis of a priority specified by the header data and the workload of the data processing processors and further argues that Locklear fails to describe or suggest a distribution processor that distributed header data, much less separated header data, at least in part on the basis of a priority specified by the header data and the workload of the data processing processors. However, the Examiner respectfully sees these arguments as misplaced. The Examiner did not rely on Kudo in answering the limitation, separating the packets into header data and useful data. The rejection clearly specifies that this limitation is taught by the Partridge reference. Kudo is referred mainly to get the

teaching on distributing data according to the priority of the header data. Locklear is referred mainly to get the teaching on distributing data according to loading characteristics of selected route processors.

Therefore, the Examiner concludes that the rejection of claims is proper.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Cho whose telephone number is 571-272-3087. The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3088.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hc
Hong Cho
Patent Examiner
09/08/2005

JOHN PEZZLO
PRIMARY EXAMINER